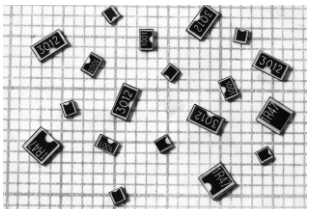
High Reliability Chip Resistors, SMD and Hybrid Application, Thick Film Technology



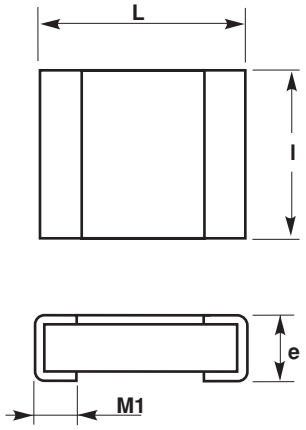
FEATURES

Two test levels are proposed:

- Level B with serialized components
- Level C without serialization
- ESA/SCC 4001 under trial test

The technology used to create these resistor chips has been developed to ensure a very high level of reproductible homogeneous and stable manufacturing process and to provide the best quality and reliability possible.
These components tested and selected for highly demanding applications, comply to the ESA/SCC 4001 specification.

DIMENSIONS in millimeters



VISHAY SFERNICE DESIGNATION	DIMENSIONS in mm				MEDIUM UNIT WEIGHT IN g
	L	l	e	M1	
CHPHR 0505	1.27 ± 0.15	1.27 ± 0.15	$^{+0.1}_{0.64-0}$	0.3 ± 0.1	0.002
CHPHR 0705	1.91 ± 0.20	1.27 ± 0.15	$^{+0.1}_{0.64-0}$	0.5 ± 0.1	0.004
CHPHR 0805	2.03 ± 0.20	1.27 ± 0.15	$^{+0.1}_{0.64-0}$	0.5 ± 0.1	0.004
CHPHR 1206	3.20 ± 0.25	1.60 ± 0.15	$^{+0.1}_{0.64-0}$	0.5 ± 0.1	0.009
CHPHR 1010	2.54 ± 0.20	2.54 ± 0.20	$^{+0.1}_{0.64-0}$	0.5 ± 0.1	0.01

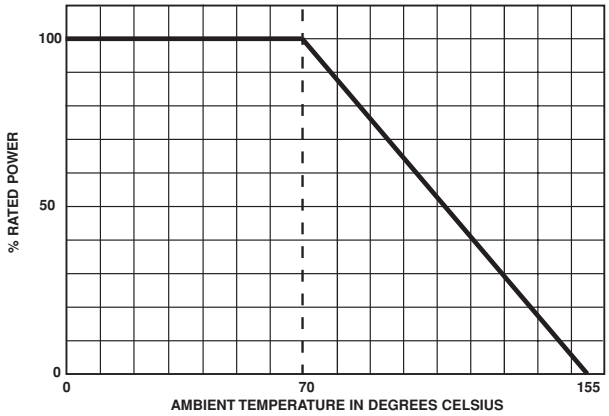
ELECTRICAL SPECIFICATIONS

VISHAY SFERNICE DESIGNATION		CHP HR 0505	CHP HR 0705	CHP HR 0805	CHP HR 1206	CHP HR 1010
ESA Specification Applied		4001/016	4001/017	4001/018	4001/020	4001/019
Power Rating at + 70°C		0.125W	0.2W	0.2W	0.25W	0.5W
Limiting Element Voltage		50V	75V	75V	150V	100V
Ohmic Values Versus Temperature Coefficient	± 100ppm/°C	> 10Ω to 1MΩ	> 10Ω to 1MΩ	> 10Ω to 1MΩ	> 10Ω to 1MΩ	> 10Ω to 1MΩ
	± 200ppm/°C	1Ω to 10Ω	1Ω to 10Ω	1Ω to 10Ω	1Ω to 10Ω	1Ω to 10Ω
Tolerance		± 1% - ± 2%				
Temperature Range		– 55°C to + 155°C				

PERFORMANCE

TESTS	CONDITIONS	LIMIT DRIFTS
Insulation Resistance	100V or 500V depend model CEI 115 - 1	1Ω G min.
Soldering (Thermal Shock)	260°C during 10 seconds CEI 68-2-20A test Tb	$\pm (0.5 + \frac{0.05\Omega}{R} \times 100)\%$
Terminal Strength	Adhesive test CEI 115 -1	$\pm (0.25 + \frac{0.05\Omega}{R} \times 100)\%$
Rapid Temperature Change	5 cycles (– 55°C + 155°C) CEI 68-2-14 test Na	$\pm (0.25 + \frac{0.05\Omega}{R} \times 100)\%$
Climatic Sequence	6 cycles, – 55°C + 155°C, 95% R.H., + 40°C, 20 mbar SCC 4001 and CEI 68-2 ...	$\pm (1 + \frac{0.05\Omega}{R} \times 100)\%$ Insulation resistance > 1000MΩ
Load Life	2000h at nominal power at + 70°C cycle 90' / 30'	$\pm (1.5 + \frac{0.05\Omega}{R} \times 100)\%$ Insulation resistance > 1000MΩ
High Temperature Exposure	2000h no load at + 155°C	$\pm (1.5 + \frac{0.05\Omega}{R} \times 100)\%$ Insulation resistance > 1000MΩ

POWER RATING CHART



TERMINATIONS

Thick film screen and fire technology is used for the wraparound termination. The film thickness is such that terminal pads play the role of stand-off and ease the cleaning process under the chip. The most common terminations used are tinned Pt Au (variant 01 : R) and the Pt Au with nickel barrier and electrotinned (variant 03 : BE).

PASSIVATION

The ruthenium oxide resistive layer is protected by a mineral passivation.

MARKING

Print marking shows: the ohmic value (4 digit code), the first three digits are significant figures and the fourth digit the number of zeros to follow.

For ohmic values less than 100 the letter R shows the position of the decimal point.

ex: 97R6 = 97.6Ω

4992 = 49900Ω

On size 0505 space available is too small and no marking is made.

PACKAGING

Chip resistors tested to level B are packaged individually in thermo sealed blisters, each blister containing 40 chips.

For chips tested to level C, we use waffle packs. The number of parts for a waffle pack depends on the size of the chips: 100 chips for sizes 0505, 0705, 0805, 1010 and 140 chips for size 1206.

On blister or waffle packs, information printed is: SFERNICE designation, the ohmic value (4 digits), the tolerance, the temperature coefficient, the manufacturing date (4 digit code), two for the year and two for the week.

ORDERING INFORMATION

CHP HR	1206	± 100ppm/°C	100Ω	± 1%	01	C1
MODEL	VERSION	TEMPERATURE COEFFICIENT	OHMIC VALUE	TOLERANCE	SCC VARIANT	QUALITY LEVEL
					01 (R)	B1 C1
					03 (BE)	B2 C2
						B3 C3